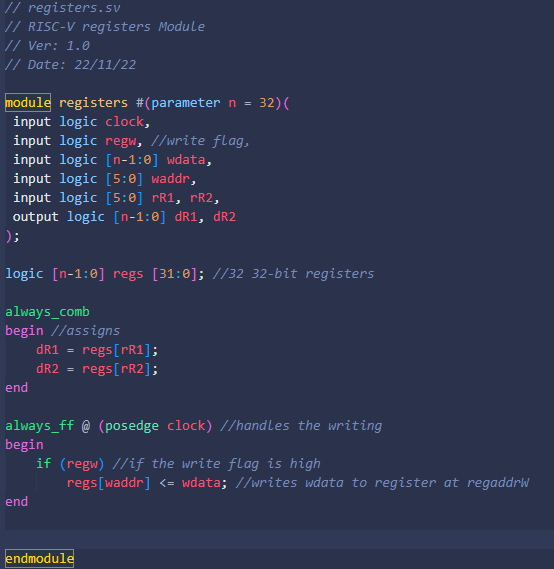
Registers Module Test

This is the code for the Registers module

The data output will be according to whatever the address input is

If regw is high the reg at waddr will be over written.



The testbench will test this.

The Test bench attempts to write when regw is high, then attempts to write when regw is low.

Then displays the value of the 2 registers at the output.

This is correctly shown in the Modelsim simulation.

10 is written to r28 and then 5000 is written to r29. Then 502 is not written to r28. This is proved at the output as dR1 = 5000 and dR2 is 10.

